

What Is Claimed Is:

1 1. A manufacturing method of a thin film transistor (TFT),
2 comprising the steps of:
3 providing a substrate;
4 depositing a conductive layer above the substrate to form
5 a gate electrode of the thin film transistor;
6 forming an insulating layer above the conductive layer and
7 the substrate;
8 sequentially forming a semiconductor layer and a doped
9 silicon layer on the insulating layer;
10 depositing a sacrifice layer with an island shape above the
11 doped silicon layer, and the sacrifice layer being positioned
12 directly above the gate electrode;
13 forming a metal layer covering the sacrifice layer and the
14 doped silicon layer;
15 patterning the metal layer to form a source electrode and
16 a drain electrode, a channel being defined between the source
17 electrode and the drain electrode, a non-TFT region being defined
18 as a portion of the substrate not covered by the source electrode,
19 the drain electrode, and the channel, and the island-shaped
20 sacrifice layer being exposed in the channel and the doped silicon
21 layer being exposed in the non-TFT region after the metal layer
22 being patterned;
23 using the source and the drain electrodes as a mask to
24 perform the following etching processes in the same time during
25 a predetermined period: (a) removing the island-shaped sacrifice
26 layer and the doped silicon layer in the channel so that the
27 semiconductor layer being exposed in the channel; and (b) removing

28 the doped silicon layer and the semiconductor layer in the non-TFT
29 region to expose the insulating layer; and
30 forming a passivation layer to cover the source electrode,
31 the drain electrode, the channel, and the substrate.

1 2. The method of claim 1, wherein during the etching process,
2 etching rates and the thickness of the island-shaped sacrifice
3 layer, the doped silicon layer, and the semiconductor layer are
4 respectively R_{IS} , T_{IS} , R_n , T_n , R_a , and T_a , and the time for removing
5 the island-shaped sacrifice layer and the doped silicon layer in
6 the channel ($T_{IS}/R_{IS} + T_n/R_n$) is not less than the time for removing
7 the doped silicon layer and the semiconductor layer in the non-TFT
8 region ($T_n/R_n + T_a/R_a$).

1 3. The method of claim 2, wherein the thickness of the
2 insulating layer in the non-TFT region is reduced by controlling
3 the thickness of the island-shaped sacrifice layer so that a
4 portion of the insulating layer is removed in the non-TFT region
5 when the island-shaped sacrifice layer and the doped silicon
6 layer is removed in the channel, and the doped silicon layer and
7 the semiconductor layer is removed in the non-TFT region.

1 4. The method of claim 3, wherein the etching rate and the
2 thickness of the removed insulating layer is R_{INS} and T_{INS} , and the
3 time for removing the sacrifice layer and the doped silicon layer
4 in the channel ($T_{IS}/R_{IS} + T_n/R_n$) is equal to the time for removing
5 the doped silicon layer, the semiconductor layer and the removed
6 insulating layer in the non-TFT region ($T_n/R_n + T_a/R_a + T_{INS}/R_{INS}$).

1 5. The method of claim 1, further comprising the following
2 steps:

3 etching the passivation layer to expose one of the source
4 electrode and the drain electrode; and

5 forming a transparent conductive layer above the
6 passivation layer so as to electrically connect to one of the
7 source electrode and the drain electrode.

1 6. The method of claim 5, wherein the semiconductor layer is
2 an amorphous silicon layer, the doped silicon layer is an n-type
3 poly-silicon layer, the conductive layer is a metal layer, the
4 substrate is made of glass or quartz, and the transparent
5 conductive layer is an indium tin oxide (ITO) layer.

1 7. A method for manufacturing a thin film transistor (TFT),
2 comprising the steps of:

3 providing a substrate;

4 depositing a conductive layer above the substrate to form
5 a gate electrode of the thin film transistor;

6 forming an insulating layer above the conductive layer and
7 the substrate;

8 forming a semiconductor layer on the insulating layer;

9 forming a sacrifice layer with an island shape on the
10 semiconductor layer, and the sacrifice layer being positioned
11 directly above the gate electrode;

12 forming a doped silicon layer on the sacrifice layer and the
13 semiconductor layer;

14 forming a metal layer covering the doped silicon layer;

15 patterning the metal layer to form a source electrode and
16 a drain electrode, a channel being defined between the source

17 electrode and the drain electrode, a non-TFT region being defined
18 as a portion of the substrate not covered by the source electrode,
19 the drain electrode and the channel, and the doped silicon layer
20 being exposed in the channel and the non-TFT region;

21 using the source and the drain electrodes as a mask to
22 perform the following etching processes at the same time during
23 a predetermined period: (a) removing the doped silicon layer and
24 the island-shaped sacrifice layer within the channel so as to
25 expose the semiconductor layer in the channel; and (b) removing
26 the doped silicon layer and the semiconductor layer in the non-TFT
27 region so as to expose the insulating layer; and

28 forming a passivation layer to cover the source electrode,
29 the drain electrode, the channel, and the non-TFT region.

1 8. The method of claim 7, wherein during the etching process,
2 the etching rate and the thickness of the island-shaped sacrifice
3 layer, the doped silicon layer, and the semiconductor layer are
4 respectively R_{IS} , T_{IS} , R_n , T_n , R_a , and T_a , and the time for removing
5 the doped silicon layer and the island-shaped sacrifice layer in
6 the channel ($T_{IS}/R_{IS} + T_n/R_n$) is not less than the time for removing
7 the doped silicon layer and the semiconductor layer in the non-TFT
8 region ($T_n/R_n + T_a/R_a$).

1 9. The method of claim 8, wherein the thickness of the
2 insulating layer in the non-TFT region is reduced by controlling
3 the thickness of the island-shaped sacrifice layer so that a
4 portion of the insulating layer is removed in the non-TFT region
5 when the doped silicon layer and the island-shaped sacrifice
6 layer is etched in the channel.

1 10. The method of claim 9, wherein the etching rate and the
2 thickness of the removed insulating layer are respectively R_{INS}
3 and T_{INS} , the time for removing the doped silicon layer and the
4 island-shaped sacrifice layer in the channel ($T_{IS}/R_{IS} + T_n/R_n$) is
5 equal to the time for removing the doped silicon layer, the
6 semiconductor layer, and the removed insulating layer in the
7 non-TFT region ($T_n/R_n + T_a/R_a + T_{INS}/R_{INS}$).

1 11. The method of claim 7, further comprising the following
2 steps:

3 etching the passivation layer to expose one of the source
4 electrode and the drain electrode; and

5 forming a transparent conductive layer above the
6 passivation layer so as to electrically connect to one of the
7 source electrode and the drain electrode.

1 12. The method of claim 11, wherein the semiconductor layer is
2 an amorphous silicon layer, the doped silicon layer is an n-type
3 poly-silicon layer, the conductive layer is a metal layer, and
4 the transparent conductive layer is an ITO layer.

1 13. A method for forming a thin film transistor liquid crystal
2 display (TFT-LCD), the TFT-LCD including at least one thin film
3 transistor (TFT) and one storage capacitor (Cs), the method
4 comprising the steps of:

5 providing a substrate;

6 depositing a first and a second conductive layer on the
7 substrate to form a gate electrode of the TFT and a bottom
8 electrode of the storage capacitor and ;

9 forming an insulating layer above the conductive layers and
10 the substrate;

11 sequentially forming a semiconductor layer and a doped
12 silicon layer on the insulating layer;

13 depositing a sacrifice layer with an island shape above the
14 doped silicon layer, and the sacrifice layer being positioned
15 directly above the first conductive layer;

16 forming a metal layer covering the sacrifice layer and the
17 doped silicon layer;

18 patterning the metal layer to form a source electrode and
19 a drain electrode above the first conductive layer, a channel
20 being defined between the source electrode and the drain
21 electrode to expose the sacrifice layer therein, and a non-TFT
22 region being defined as a portion of the substrate not covered
23 by the source electrode, the drain electrode, and the channel so
24 as to expose the doped silicon layer thereon;

25 using the source and the drain electrodes as a mask to
26 perform the following etching processes at the same time (a) to
27 remove the island-shaped sacrifice layer and the doped silicon
28 layer in the channel, as well as (b) to remove the doped silicon
29 layer and the semiconductor layer in the non-TFT region, so that
30 the semiconductor layer being exposed in the channel and the
31 insulating layer being exposed in the non-TFT region; and

32 forming a passivation layer to cover the source electrode,
33 the drain electrode, the channel, and the second conductive
34 layer.

1 14. The method of claim 13, wherein during the etching process,
2 etching rates of the island-shaped sacrifice layer, the doped
3 silicon layer, and the semiconductor layer are respectively R_{1s} ,

4 R_n and R_a , the thickness of the island-shaped sacrifice layer, the
5 doped silicon layer, and the semiconductor layer are respectively
6 T_{IS} , T_n , and T_a , and the time for removing the island-shaped
7 sacrifice layer and the doped silicon layer in the channel (T_{IS}/R_{IS}
8 $+ T_n/R_n$) is not less than the time for removing the doped silicon
9 layer and the semiconductor layer in the non-TFT region ($T_n/R_n +$
10 T_a/R_a).

1 15. The method of claim 14, wherein the thickness of the
2 insulating layer in the non-TFT region is reduced by controlling
3 the thickness of the island-shaped sacrifice layer so that a
4 portion of the insulating layer is removed in the non-TFT region
5 when the island-shaped sacrifice layer and the doped silicon
6 layer is removed in the channel, and the doped silicon layer and
7 the semiconductor layer is removed in the non-TFT region.

1 16. The method of claim 15, wherein the etching rate and the
2 thickness of the removed insulating layer are R_{INS} and T_{INS} , and the
3 time for removing the island-shaped sacrifice layer and the doped
4 silicon layer in the channel ($T_{IS}/R_{IS} + T_n/R_n$) is equal to the time
5 for removing the doped silicon layer, the semiconductor layer,
6 and the removed insulating layer in the non-TFT region ($T_n/R_n +$
7 $T_a/R_a + T_{INS}/R_{INS}$).

1 17. The method of claim 13, further comprising the following
2 steps:

3 forming a hole in the passivation layer to expose one of the
4 source electrode and the drain electrode; and

5 depositing a transparent conductive layer above the
6 passivation layer and extending above one of the source and drain

7 electrodes and the second conductive layer, and the transparent
8 conductive layer being electrically connected to one of the
9 source and drain electrodes through the hole for forming an upper
10 electrode of the storage capacitor.

1 18. A method for forming a thin film transistor liquid crystal
2 display (TFT-LCD), the TFT-LCD having at least one thin film
3 transistor (TFT) and one storage capacitor (Cs), the method
4 comprising the steps of:
5 providing a substrate;
6 depositing a first conductive layer and a second conductive
7 layer above the substrate to form a gate electrode of the TFT and
8 a bottom electrode of the storage capacitor;
9 forming an insulating layer on the first and second
10 conductive layers and the substrate;
11 depositing a semiconductor layer and a doped silicon layer
12 on the insulating layer;
13 forming a sacrifice layer with an island shape on the doped
14 silicon layer, and the sacrifice layer being positioned directly
15 above the first conductive layer;
16 forming a metal layer covering the sacrifice layer and the
17 doped silicon layer;
18 patterning the metal layer to form a source electrode and
19 a drain electrode above the first conductive layer as well as to
20 form a shielding metal layer above the second conductive layer,
21 a channel being defined between the source electrode and the drain
22 electrode to expose the sacrifice layer in the channel, a
23 capacitor region being defined as a portion of the substrate
24 covered by the shielding metal layer, and a non-TFT region being
25 defined as a portion of the substrate not covered by the source

26 electrode, the drain electrode, the capacitor region, and the
27 channel so as to exposed the doped silicon layer thereon;

28 using the source electrode, the drain electrode, and the
29 shielding metal layer as a mask to perform the following etching
30 processes at the same time: (a) removing the doped silicon layer
31 and the island-shaped sacrifice layer in the channel so as to
32 expose the semiconductor layer therein, and (b) removing the
33 doped silicon layer and the semiconductor layer in the non-TFT
34 region so as to expose the insulating layer thereon; and

35 forming a passivation layer to cover the source electrode,
36 the drain electrode, the channel, and the capacitor region.

1 19. The method of claim 18, wherein during the etching process,
2 etching rates of the island-shaped sacrifice layer, the doped
3 silicon layer, and the semiconductor layer are R_{IS} , R_n , and R_a
4 respectively, the thickness of the island-shaped sacrifice
5 layer, the doped silicon layer, and the semiconductor layer are
6 T_{IS} , T_n , and T_a , and the time for removing the island-shaped
7 sacrifice layer and the doped silicon layer in the channel (T_{IS}/R_{IS}
8 + T_n/R_n) is not less than the time for removing the doped silicon
9 layer and the semiconductor layer in the non-TFT region (T_n/R_n +
10 T_a/R_a).

1 20. The method of claim 18 further comprising the following
2 steps:

3 patterning the passivation layer to form a first hole and
4 a second hole so as to expose one of the source electrode and
5 the drain electrode through the first hole, and expose the
6 shielding metal layer in the capacitor region through the second
7 hole; and

8 forming a transparent conductive layer above the
9 passivation layer, the transparent conductive layer being
10 electrically connected to one of the source and the drain
11 electrodes through the first hole, as well as electrically
12 connected to the shielding metal layer through the second hole
13 for forming an upper electrode of the storage capacitor.

1 21. A method for manufacturing a thin film transistor liquid
2 crystal display (TFT-LCD), the TFT-LCD having at least one thin
3 film transistor (TFT) and one storage capacitor (Cs), the method
4 comprising the steps of:

5 providing a substrate;

6 depositing a first and a second conductive layer above the
7 substrate to form a gate electrode of the TFT and a bottom
8 electrode of the storage capacitor, respectively;

9 forming an insulating layer above the conductive layers and
10 the substrate;

11 depositing a semiconductor layer on the insulating layer;

12 forming a sacrifice layer with an island shape on the
13 semiconductor layer, and the sacrifice layer being positioned
14 directly above the first conductive layer;

15 depositing a doped silicon layer on the island-shaped
16 sacrifice layer and the semiconductor layer;

17 forming a metal layer covering the doped silicon layer and
18 the island-shaped sacrifice layer;

19 patterning the metal layer to form a source electrode and
20 a drain electrode above the first conductive layer, a channel
21 being defined between the source electrode and the drain
22 electrode to expose the doped silicon layer therein, and a non-FT
23 region being defined as a portion of the substrate not covered

24 by the source electrode, the drain electrode, and the channel to
25 expose the doped silicon layer thereon;

26 using the source and the drain electrodes as a mask to
27 perform the following etching processes at the same time to (a)
28 remove the doped silicon layer and the island-shaped sacrifice
29 layer in the channel so as to expose the semiconductor layer in
30 the channel, and (b) to remove the doped silicon layer and the
31 semiconductor layer in the non-TFT region so as to expose the
32 insulating layer; and

33 forming a passivation layer to cover the source electrode,
34 the drain electrode, the channel, and the second conductive
35 layer.

1 22. The method of claim 21, wherein during the etching process,
2 the etching rate and the thickness of the island-shaped sacrifice
3 layer, the doped silicon layer, and the semiconductor layer are
4 R_{IS} , T_{IS} , R_n , T_n , R_a , and T_a respectively; and the time for removing
5 the doped silicon layer and the island-shaped sacrifice layer in
6 the channel ($T_{IS}/R_{IS} + T_n/R_n$) is not less than the time for removing
7 the doped silicon layer and the semiconductor layer in the non-TFT
8 region ($T_n/R_n + T_a/R_a$).

1 23. The method of claim 22, wherein the thickness of the
2 insulating layer in the non-TFT is reduced by controlling the
3 thickness of the island-shaped sacrifice layer so that a portion
4 of the insulating layer is removed in the non-TFT region when the
5 doped silicon layer and the island-shaped sacrifice layer in the
6 channel is etched away.

1 24. The method of claim 23, wherein the etching rate and the
2 thickness of the removed insulating layer are R_{INS} and T_{INS} , and the
3 time for removing the doped silicon layer and the island-shaped
4 sacrifice layer in the channel ($T_{IS}/R_{IS} + T_n/R_n$) is equal to the time
5 for removing the doped silicon layer, the semiconductor layer,
6 and the removed insulating layer in the non-TFT region ($T_n/R_n +$
7 $T_a/R_a + T_{INS}/R_{INS}$).

1 25. The method of claim 21 further comprising the following
2 steps:

3 forming a hole in the passivation layer to expose one of the
4 source and drain electrodes; and

5 depositing a transparent conductive layer above the
6 passivation layer so as to electrically connect to one of the
7 source and drain electrodes through the hole.

1 26. A method for manufacturing a thin film transistor liquid
2 crystal display (TFT-LCD), the TFT-LCD having at least one thin
3 film transistor (TFT) and one storage capacitor, the method
4 comprising the steps of:

5 providing a substrate;

6 depositing first and second conductive layers above the
7 substrate to respectively form a gate electrode of the TFT and
8 a bottom electrode of the storage capacitor;

9 forming an insulating layer above the first and second
10 conductive layers and the substrate;

11 forming a semiconductor layer on the insulating layer;

12 forming a sacrifice layer with an island shape on the
13 semiconductor layer, and the sacrifice layer being positioned
14 directly above the first conductive layer;

15 depositing a doped silicon layer to cover the sacrifice
16 layer and the semiconductor layer;

17 forming a metal layer covering the doped silicon layer;

18 patterning the metal layer to form a source electrode and
19 a drain electrode above the first conductive layer, as well as
20 to form a shielding metal layer above the second conductive layer;
21 a channel being defined between the source electrode and the drain
22 electrode to expose the doped silicon layer therein; a capacitor
23 region being defined as a portion of the substrate covered by the
24 shielding metal layer; and a non-TFT region being defined as the
25 substrate not covered by the source electrode, the drain
26 electrode, the capacitor, and the channel so as to expose the
27 doped silicon layer thereon;

28 using the source and drain electrodes and the shielding
29 metal layer as a mask to perform these etching processes at the
30 same time: (a) removing the doped silicon layer and the
31 island-shaped sacrifice layer in the channel so as to expose the
32 semiconductor layer in the channel, and (b) removing the doped
33 silicon and semiconductor layers in the non-TFT region to expose
34 the insulating layer therein; and

35 forming a passivation layer to cover the source electrode,
36 the drain electrode, the channel, and the capacitor region.

1 27. The method of claim 26, wherein during the etching process,
2 etching rates of the island-shaped sacrifice layer, the doped
3 silicon layer, and the semiconductor layer are R_{IS} , R_n , and R_a
4 respectively; the thickness of the island-shaped sacrifice
5 layer, the doped silicon layer, and the semiconductor layer are
6 T_{IS} , T_n , and T_a ; and the time for removing the doped silicon layer
7 and the island-shaped sacrifice layer in the channel ($T_{IS}/R_{IS} +$

8 T_n/R_n) is not less than the time for removing the doped silicon
9 layer and the semiconductor layer in the non-TFT region ($T_n/R_n +$
10 T_a/R_a) .

1 28. The method of claim 27 further comprising the following
2 steps:

3 forming a first hole and a second hole in the passivation
4 layer so as to expose one of the source and drain electrodes via
5 the first hole, and expose the shielding metal layer via the
6 second hole; and

7 forming a transparent conductive layer above the
8 passivation layer, the transparent conductive layer being
9 electrically connected to one of the source electrode and the
10 drain electrode through the first hole, as well as electrically
11 connected to the shielding metal through the second hole for
12 forming an upper electrode of the storage capacitor.

1 29. A thin film transistor (TFT), comprising:
2 a gate electrode with an island shape formed on a substrate;
3 an insulating layer covering the gate electrode;
4 a semiconductor layer with an island shape formed on the
5 insulating layer, and positioned directly above the gate
6 electrode;
7 a source doped silicon layer and a drain doped silicon layer
8 formed on the semiconductor layer, a channel being defined
9 between the source doped silicon layer and the drain doped silicon
10 layer to expose the semiconductor layer therein;
11 first and second sacrifice layers with island shapes
12 respectively formed on the source doped silicon layer and drain

13 doped silicon layer, the first and the second sacrifice layers
14 being spaced apart by the channel;
15 a source electrode formed above the first sacrifice layer
16 and the source doped silicon layer; and
17 a drain electrode formed above the second sacrifice layer
18 and the drain doped silicon layer;
19 wherein the thickness of the first and second sacrifice
20 layers varies according to the thickness of the semiconductor
21 layer because the time for etching the first and second sacrifice
22 layers is substantially equal to the time for etching the
23 semiconductor layer in the subsequent process.

1 30. The TFT in claim 29, wherein during the etching process, the
2 etching rate of the first and the second sacrifice layers is R_{IS} ,
3 the etching rate and the thickness of the drain doped silicon and
4 the source doped silicon layers are R_n and T_n , and the etching rate
5 and the thickness of the semiconductor layer are R_a and T_a , and
6 the thickness of the first and the second sacrifice layers T_{IS}
7 meets the equation of $(T_{IS}/R_{IS} + T_n/R_n) \geq (T_n/R_n + T_a/R_a)$.

1 31. The TFT in claim 29, further comprising a passivation layer
2 covering the source electrode, the drain electrode, and the
3 channel, and the TFT is used in an in-plane-switch (IPS) type LCD.

1 32. The TFT in claim 29, further comprising:
2 a passivation layer covering the TFT on the substrate, and
3 having a hole above the drain electrode; and
4 a transparent conductive layer formed above the drain
5 electrode and electrically connected to the drain electrode via
6 the hole.

1 33. A thin film transistor (TFT), comprising:

2 a gate electrode with an island shape formed on a substrate;
3 an insulating layer covering the gate electrode;

4 a semiconductor layer with an island shape formed on the
5 insulating layer, and positioned above the gate electrode;

6 first and second sacrifice layers with island shapes formed
7 on the semiconductor layer, and a channel being defined between
8 the first and second sacrifice layers so as to expose the
9 semiconductor layer;

10 a source doped silicon layer and a drain doped silicon layer
11 formed above the first sacrifice layer, second sacrifice layer,
12 and the semiconductor layer, the source doped silicon layer and
13 the drain doped silicon layer being spaced apart by the channel;
14 and

15 a source electrode and a drain electrode respectively formed
16 on the source doped silicon layer and the drain doped silicon
17 layer;

18 wherein the thickness of the first and second sacrifice
19 layers varies with the thickness of the semiconductor layer
20 because the time for etching the first and second sacrifice layers
21 is substantially equal to the time for etching the semiconductor
22 layer in the subsequent process.

1 34. The TFT in claim 33, wherein the etching rate of the first
2 and the second island-shaped sacrifice layers is R_{is} , the etching
3 rate and the thickness of the drain doped silicon and the source
4 doped silicon layers are R_n and T_n , the etching rate and the
5 thickness of the island-shaped semiconductor layer are R_a and T_a ,
6 and the thickness of the first and the second island-like

7 sacrifice layers T_{is} meets the equation of $(T_{is}/R_{is} + T_n/R_n) \geq (T_n/R_n$
8 $+ T_a/R_a)$.

1 35. The TFT in claim 33, further comprising a passivation layer
2 covering the source electrode, the drain electrode, and the
3 channel, and the TFT is used in an in-plane-switch (IPS) type LCD.

1 36. The TFT in claim 33 further comprising:
2 a passivation layer covering the TFT on the substrate, and
3 having a hole above the drain electrode; and
4 a transparent conductive layer formed above the drain
5 electrode and electrically connected to the drain electrode via
6 the hole.